ABSTRACT OF THE DISCLOSURE

A method of fabricating a semiconductor device having a metal gate pattern is provided in which capping layers are used to control the relative oxidation rates of portions of the metal gate pattern during a oxidation process. The capping layer may be a multilayer structure and may be etched to form insulating spacers on the sidewalls of the metal gate pattern. The capping layer(s) allow the use of a selective oxidation process, which may be a wet oxidation process utilizing partial pressures of both H_2O and H_2 in an H_2-rich atmosphere, to oxidize portions of the substrate and metal gate pattern while suppressing the oxidation of metal layers that may be included in the metal gate pattern. This allows etch damage to the silicon substrate and edges of the metal gate pattern to be reduced while substantially maintaining the original thickness of the gate insulating layer and the conductivity of the metal layer(s).